48 V-to-PoL POWER STAMP DC-DC CONVERTER

For Open Compute Project® & Data Center Applications

Intel® VR13. and VR13.HC CPUs
DDR4 memory
IBM® POWER9™

POWER STAMP ALLIANCE

Direct Conversion From 48 V or 54 V Bus

OCP® Servers for Data Centers

Communication Systems

Storage and Data Processing Equipment

Low Voltage, High Current ASICs and FPGAs

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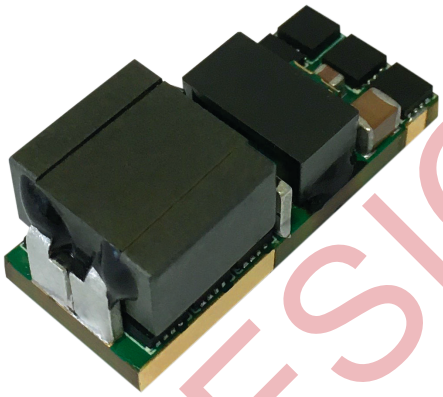
48 V-to-PoL Power Stamp DC-DC Converter

The MAIN and SATELLITE Power Stamp are isolated DC-DC converters housed in an industry standard form factor defined by the Power Stamp Alliance. They convert a 48 V bus voltage into a low voltage suitable for typical server's motherboard subsystems.

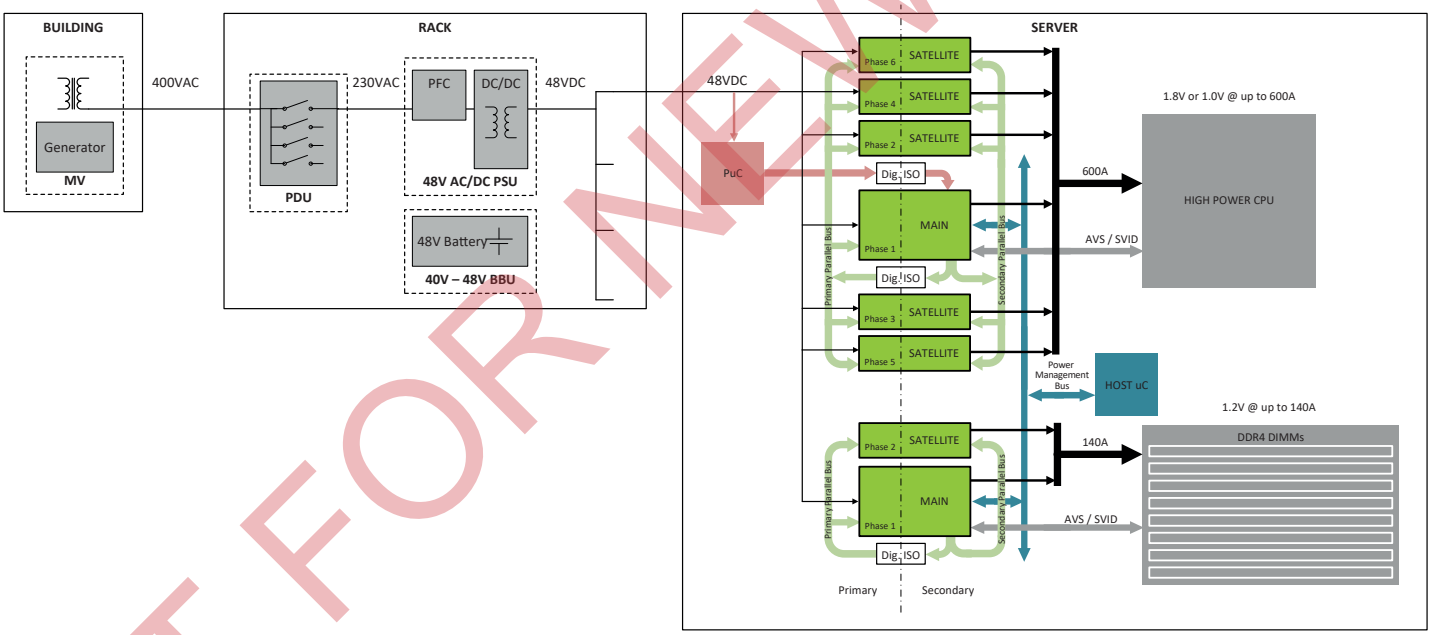
Key Features

- **Over 94% peak efficiency at 1.8 Vout**
- **Over 91% peak efficiency at 1.0 Vout**
- Up to 140 W continuous output power / 200 W peak
- Up to 70 A continuous output current / 100 A peak
- Wide 40 V to 60 V input voltage range
- Power density exceeding 300 W/in^3
- Parallel up to six "stamps" with automatic phase shedding
- Flat efficiency curve over wide load ranges
- Source and sink mode for fast transient response
- Isolated power train
- Secondary side fully digital control
- Power Management Bus with configurable AVSBus® or Intel® SVID interface



From 48 V to Point of Load

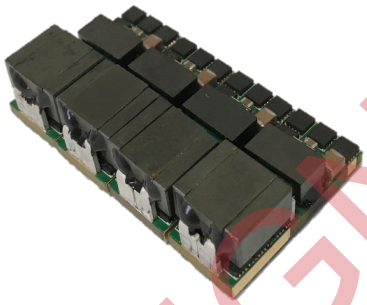
Emerging data center architectures enable higher efficiencies at the system level, directly translating into lower operating costs and lower total cost of ownership.



New power distribution architectures are eliminating centralized UPS systems and 12 V power distribution busses in cabinet racks by means of higher voltage busses – typically 48 V or 54 V – and distributed battery backup units. Higher power densities, drastically lower power distribution losses and simplified battery management are achieved at the expense of more complex voltage regulators on server's motherboards. The increased voltage gap poses new challenges not simply addressed by traditional multi-phase buck regulators. Although isolation is not strictly a requirement, single stage, isolated topologies provide an effective solution to this new power conversion dilemma.

The Power Stamp Form Factor

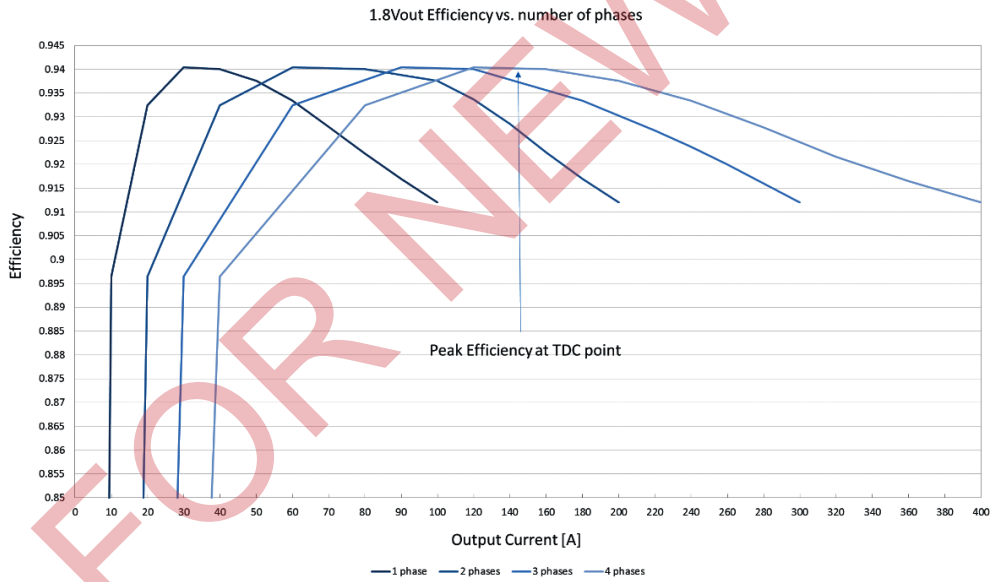
The SATELLITE Power Stamp is the basic building block for large DC-DC converter subsystems featuring scalable output power and efficiency. The SATELLITE is an isolated power train based on a proprietary phase shifted full bridge topology. It is part of a family of industry-standard products defined by the Power Stamp Alliance. The STPSA60 is an IC controller and can drive multi-phase arrays of up to six paralleled SATELLITEs.



The MAIN Power Stamp – which include one SATELLITE power train and the STPSA60 controller in the same Power Stamp form factor – provides a pre-configured, fully integrated, voltage regulator with even higher power density and ease of use. As the STPSA60 controller, the MAIN Power Stamp can drive arrays of up to six phases – one of which is on-board enabling also standalone configurations. Power Stamps are available with input voltage range compliant with OCP specifications, output voltages suitable for typical server's motherboards subsystems and are made using high volume low cost manufacturing techniques.

Scalable Efficiency

The multi-phase buck converter is the industry workhorse for what concerns low voltage, high current applications. If practical duty cycles are considered, the buck topology is however most effective in applications with small input to output voltage differences. The Power Stamp architecture fills the voltage difference gap with a topology that is intrinsically equivalent to the buck converter without its duty cycle limitations. Advanced digital control with embedded Power Management Bus, telemetry and CPU-link interface - either Intel® SVID or Power Management Bus AVSBus® – supported by a simple GUI and software tools, facilitates rapid applications development. Interleaving among phases with active current balancing and dynamic phase-management with automatic phase shedding allows power system architects to design efficiency-optimized applications from low loads up to extremely high output currents. Power Stamps provide the same scalability of legacy buck converters with the additional benefits of isolated topologies at minimal system complexity. The secondary side control connects with the primary with inexpensive and easy to use digital isolators, thus limiting the risks associated with failures in high-voltage, high-energy areas of the system.



Power Stamp Model Selection

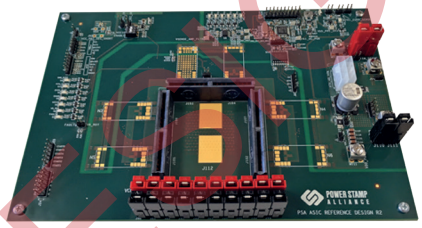
PART NUMBER	INPUT VOLTAGE [V]	OUTPUT VOLTAGE * [V]	OUTPUT CURRENT [A]	OUTPUT CURRENT [A PEAK]	EFFICIENCY (TYPICAL)
MAIN Power Stamps					
ST4-1V8M07xx	40 – 60	1.6 – 2.0	70	100	94%
ST4-1V2M07xx	40 – 60	1.16 – 1.26	70	100	91.6%
ST4-1V0M07xx	40 – 60	0.9 – 1.1	70	100	91%
SATELLITE Power Stamps					
ST4-1V8S07xx	40 – 60	1.6 – 2.0	70	100	94%
ST4-1V2S07xx	40 – 60	1.16 – 1.26	70	100	91.6%
ST4-1V0S07xx	40 – 60	0.9 – 1.1	70	100	91%
Controller IC					
STPSA60	–	–	–	–	–

* Output voltage range of typical applications - Contact factory for NVM configuration files for different output voltage settings.

Reference Designs

Evaluation boards are available to help customers with the development of a wide range of applications. Reference designs from both Intel® Xeon® and IBM® POWER9™ CPU families are addressed by pre-configured arrays of Power Stamp modules and CPU sockets. Board layouts and bulk capacitor banks are strictly following CPU manufacturer's guidelines for accurate and repeatable results.

The ASICs Evaluation Board can easily model and apply custom load profiles specified by sub-micron ASICs and FPGAs manufacturers. It features high current, low impedance socket connections to LoadSlammer's and is configurable for any Power Stamp output voltage and array size. Where applicable, Evaluation Boards can use an on-board MAIN Power Stamp or the included STPSA60 Controller and SATELLITEs, for maximum flexibility in the configuration of the Power Stamp array. Isolated or non-isolated configurations are alternatively supported with simple jumper settings.



Evaluation Boards

ARCHITECTURE	FAMILY	RELEASE DATE	TDP	SOCKET	MODULE TYPE (NUMBER)	PART NUMBER
Skylake	Xeon®	Q3/2017	140 – 205 W	Socket P	SATELLITE (3) + STPSA60	ST4-1V8S07E1
Cascade Lake	Xeon®	2018	165 – 205 W	Socket P	SATELLITE (3) + STPSA60	ST4-1V8S07E1
Ice Lake	Xeon®	2018 / 2019	Up to 230 W	Socket P+	MAIN / STPSA60 + SATELLITE (3)	ST4-1V8M07E2
ASICs	–	H1/2019	Up to 600 W	Mini Slammer / LoadSlammer	MAIN + SATELLITE (5)	ST4-1VxM07E3*
LaGrange	POWER9™	H2/2019	–	FC-PLGA	–	ST4-1V0M07E4

* x = Output voltage of installed Power Stamp modules

POWER STAMP ALLIANCE

The Power Stamp Alliance defines a standard product footprint and functions that provide a multiple-sourced, standard board-mounted solution for power conversion for 48 Vin to low voltage, high current applications. These 48 V direct conversion DC-DC modules - or 'power stamps' - primarily target devices used in large data centers (CPU, DDR, FPGA, ASIC), many of which are following the principles of the Open Compute Project® (OCP). Some of the first processor architectures addressed by the Power Stamp Alliance are the Intel® VR13. Skylake CPUs, Intel® VR13.HC Ice Lake CPUs, DDR4 memories, IBM® POWER9™ architecture processors and devices using the Power Management Bus with AVSBus® protocol or SVID protocol.

48 V single stage power conversion offers Open Compute Project® and data center companies a range of business and technical benefits.

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